REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated March 13, 2003 have been carefully reviewed by the Applicants. The Applicants thank the Examiner for the allowance of Claims 36-45. A declaration executed under 47 CFR 1.132 by a named inventor in the application is attached in support of arguments against the rejection of Claims 29-35 and 46-48.

Claims 29-30, 32-34, and 46 are currently rejected under 35 U.S.C. 103(a) as being unpatentable over Thei et al. (US 6350662) in view of Wolf et al. (Silicon Processing for the VLSI Era Volume 1: Process Technology, Lattice Press, Sunset Beach, CA USA pp. 218-19, 228, 1986). Applicants respectfully traverse the rejection on the grounds that a motive to combine the teachings of Thei and Wolf is lacking.

The rejection holds that:

> Wolf et al. discloses low temperature techniques for forming SiO_2 by CVD page 219. Also at processing temperatures less than 800°, stress at corners of SiO_2 is not large enough to cause plastic deformation (i.e., defect formation).

The disclosure of forming SiO_2 by CVD on page 219 is as follows:

> ...as with other low temperature techniques for preparing SiO_2 (CVD, PECVD) these plasma oxidized films have inferior electrical properties compared to thermal SiO_2 grown at 1000° C. Note that these properties can be substantially improved by post-oxide thermal treatment in an oxidizing ambient.

The teaching on page 219 does not provide a motivation to replace thermally grown SiO_2 or HPCVD with low temperature CVD, since the low temperature SiO_2 is described as inferior on page 219. On page 228, Wolf teaches:

As for the motivation to use low temperature CVD because of corner stress, it should be noted that the teaching of Wolf on page 228 is with respect to stress at a corner in a window cut into an SiO_2 film:

> The stress at the corner of a window cut into the oxide can be sufficiently large to induce plastic deformation in the silicon at processing temperatures above 1000° C.

An SiO_2 film on a planar silicon substrate will have a very sharp, well defined interface between the film and the substrate. A window cut into the SiO_2 film will produce a sharp corner at the substrate surface. The present invention does not involve a window cut into an SiO_2 film, and the only relevant "corner" is the corner of a trench. The corner of a trench produced by etching may have a sharp corner prior to oxidation, but the thermal oxidation process will round off the sharp corner of the silicon.

The stress discussed by Wolf on page 228 is the result of a highly undesirable geometry compounding a thermal mismatch upon an increase in temperature, that is, cut a window in an SiO_2 film on a substrate and heat the film and substrate. An example of such a process is opening an implant window, implanting a dopant, and annealing.

The motivation provided by Wolf on page 228 is to avoid heating silicon substrates with windowed SiO_2 films above 800° C. The stress produced by heating a substrate with a windowed film would be largely independent of the deposition process used to produce the film, and is primarily determined by the window corner geometry and the thermal mismatch between the silicon substrate and the SiO_2 film.

There is no window present in the thermally grown oxide film of Thei, and on page 228, Wolf only discusses stress as being a problem for a film with a window that is heated above 800° C. It should be noted that opening of a window is typically done in the presence of a photoresist, and is thus done at a relatively low temperature. On page 228, Wolf teaches that "When the stress in a thermally grown SiO_2 film is measured at room temperature it is found to be compressive and to have a relatively small magnitude. There is nothing in Wolf on page 228 to suggest that a low temperature CVD film would have any particular benefit.

The sole teaching of Wolf respect to a low temperature CVD SiO_2 film is that it has inferior electrical properties to a thermally grown film, and that it can be substantially improved by post oxide thermal treatment. In isolation trenches, SiO_2 is used to provide electrical isolation. In light of the teachings of Wolf and Thei, one with normal skill in the art would not replace the HDPCVD film of Thei with the low temperature CVD film of Wolf.

As discussed previously, Thei teaches a HDPCVD process for depositing the trench oxide fill. HDP equipment is not designed for producing thermally grown and annealed films. This limitation of HDP equipment is affirmed in the attached declaration executed by an inventor named in the present application (Krishnaswamy Ramkumar). Since the process of thermally growing and annealing an oxide film would not be feasible using currently available HDP equipment, the method of Thei thus entails an excursion to room temperature between the liner oxide anneal and trench fill.

As shown in Figure 5 of the present application, and described at page 13, lines 19-20, in step 540, the substrate temperature is reduced from the anneal temperature of 1050 degrees to 800 degrees for further processing, e.g., the CVD deposition of the silicon dioxide trench filler (page 12, lines 21-23). This sequence cannot be done in accordance with the process of Thei.

To further clarify the difference between Thei and claim 29, "decreasing the temperature of said substrate from said second temperature to a third temperature" has been amended to recite "monotonically decreasing the temperature of said substrate from said second temperature to a third temperature."

Claims 31, 35, 47, and 48 are currently rejected under 35 U.S.C. 103(a) as being unpatentable over Thei et al. and Wolf et al. , as applied above and further in view of Olsen et al. (US 6150234). Applicants respectfully traverse the rejection on the grounds that a motive to combine the teachings of Thei and Wolf is lacking, as explained above.

It is also significant that Olsen, in agreement with Thei, teaches that a HDP oxide trench fill be used (column 4, lines 18-20). Thei and Olsen both teach the use of HDP oxide as a trench fill, and thus an associated excursion to room temperature after anneal. Wolf has nothing in particular to say with respect to SiO_2 used as a trench fill and denigrates low temperature SiO_2, saying that low temperature SiO_2 is inferior. In view of Olsen, the motive to combine Thei with Wolf is further removed, as Olsen teaches the same trench fill as Thei.

In summary, Applicants assert that Claims 29-35 and 46-48 are in condition for allowance and earnestly solicit such action by the Examiner.

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Respectfully submitted,

WAGNER, MURABITO & HAO

Date: November 24, 2003

Mehlin Dean Matthews
Registration Number: 46,127

WAGNER, MURABITO & HAO
Two North Market Street
Third Floor
San Jose, CA 95113

408-938-9060